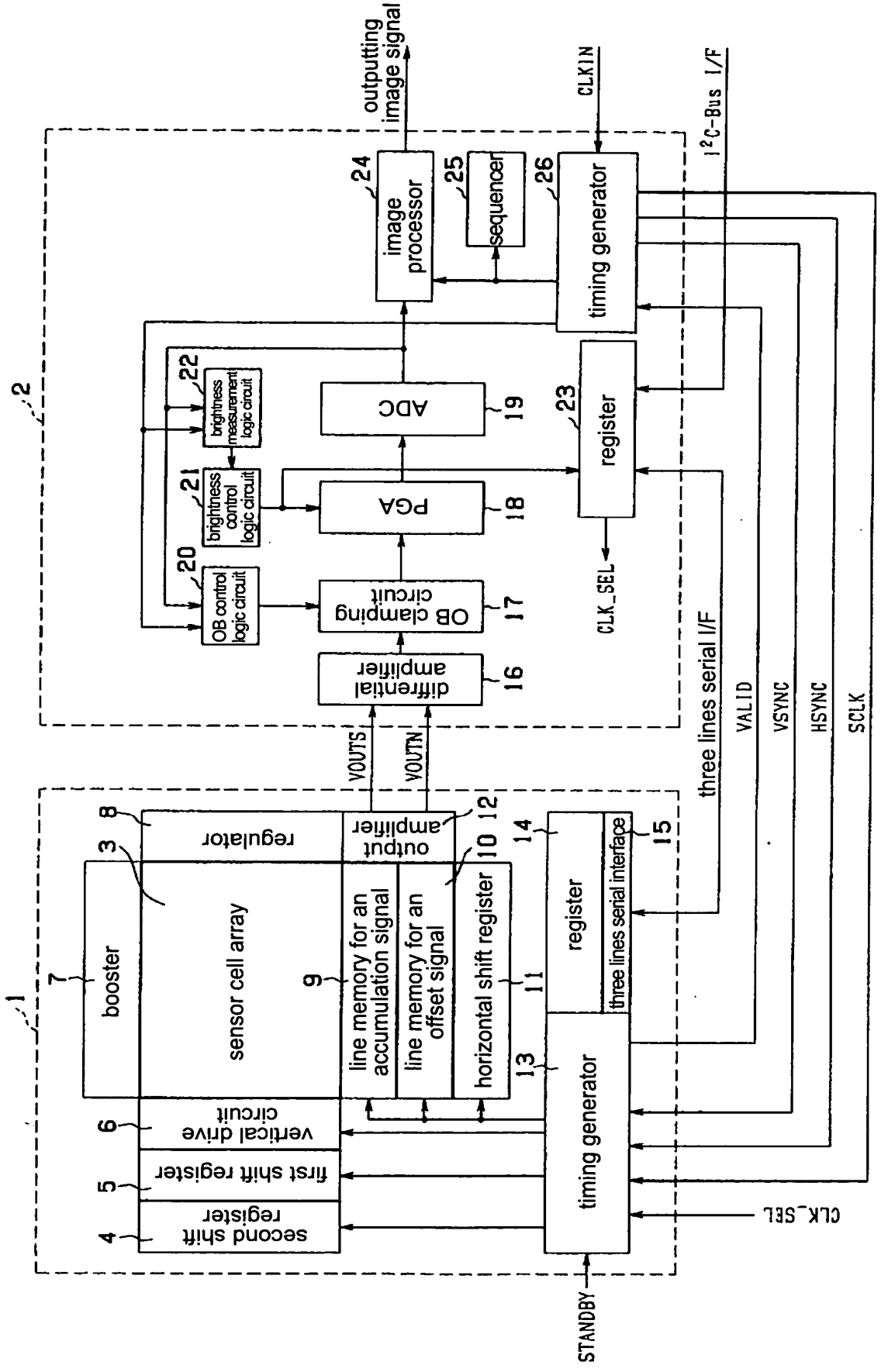
outputting image signal
CLKIN
I²C-Bus I/F
image processor
sequencer
timing generator
ADC
register
brightness measurement logic circuit
brightness control logic circuit
PGA
OB control logic circuit
OB clamping circuit
differential amplifier
CLK_SEL
three lines serial I/F
VALID
VSYNC
HSYNC
SCLK
VOUTS
VOUTN
regulator
output amplifier
booster
sensor cell array
line memory for an accumulation signal
line memory for an offset signal
horizontal shift register
register
three lines serial interface
vertical drive circuit
first shift register
second shift register
timing generator
CLK_SEL
STANDBY

FIG. 1

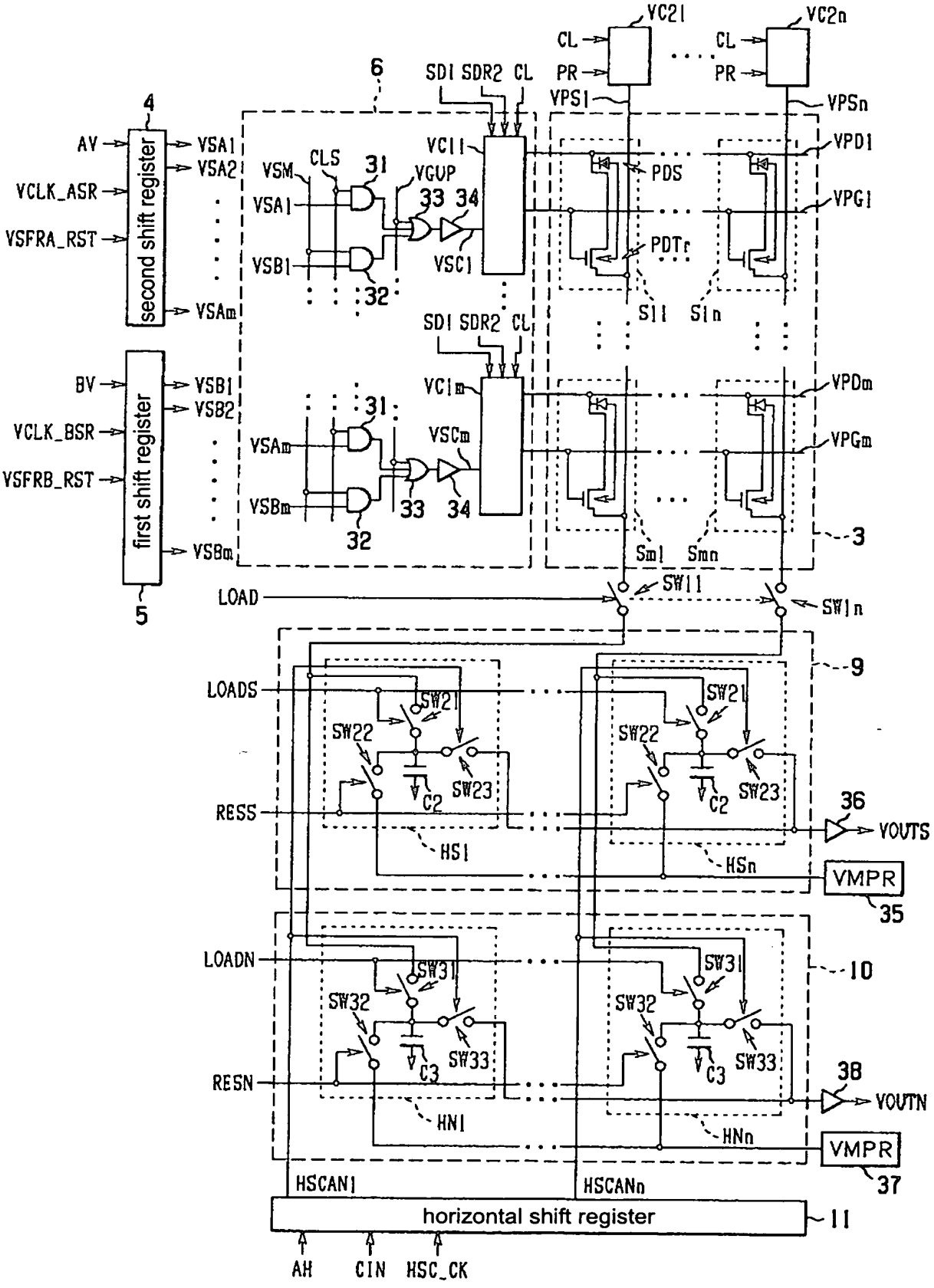
second shift register
first shift register
horizontal shift register
AV
VCLK_ASR
VSFRA_RST
BV
VCLK_BSR
VSFRB_RST
VSA1
VSA2
VSAm
VSB1
VSB2
VSBm
VSM
CLS
VGUP
VC11
VC1m
VC21
VC2n
SDI SDR2 CL
CL
PR
VPS1
VPSn
VPD1
VPDm
VPG1
VPGm
PDS
PDTr
S11
S1n
Sm1
Smn
LOAD
SW11
SW1n
LOADS
LOADN
RESS
RESN
SW21
SW22
SW23
SW31
SW32
SW33
C2
C3
HS1
HSn
HN1
HNn
VOUTS
VOUTN
VMPR
HSCAN1
HSCANn
AH
CIN
HSC_CK
3
4
5
6
9
10
11
31
32
33
34
35
36
37
38

FIG. 2

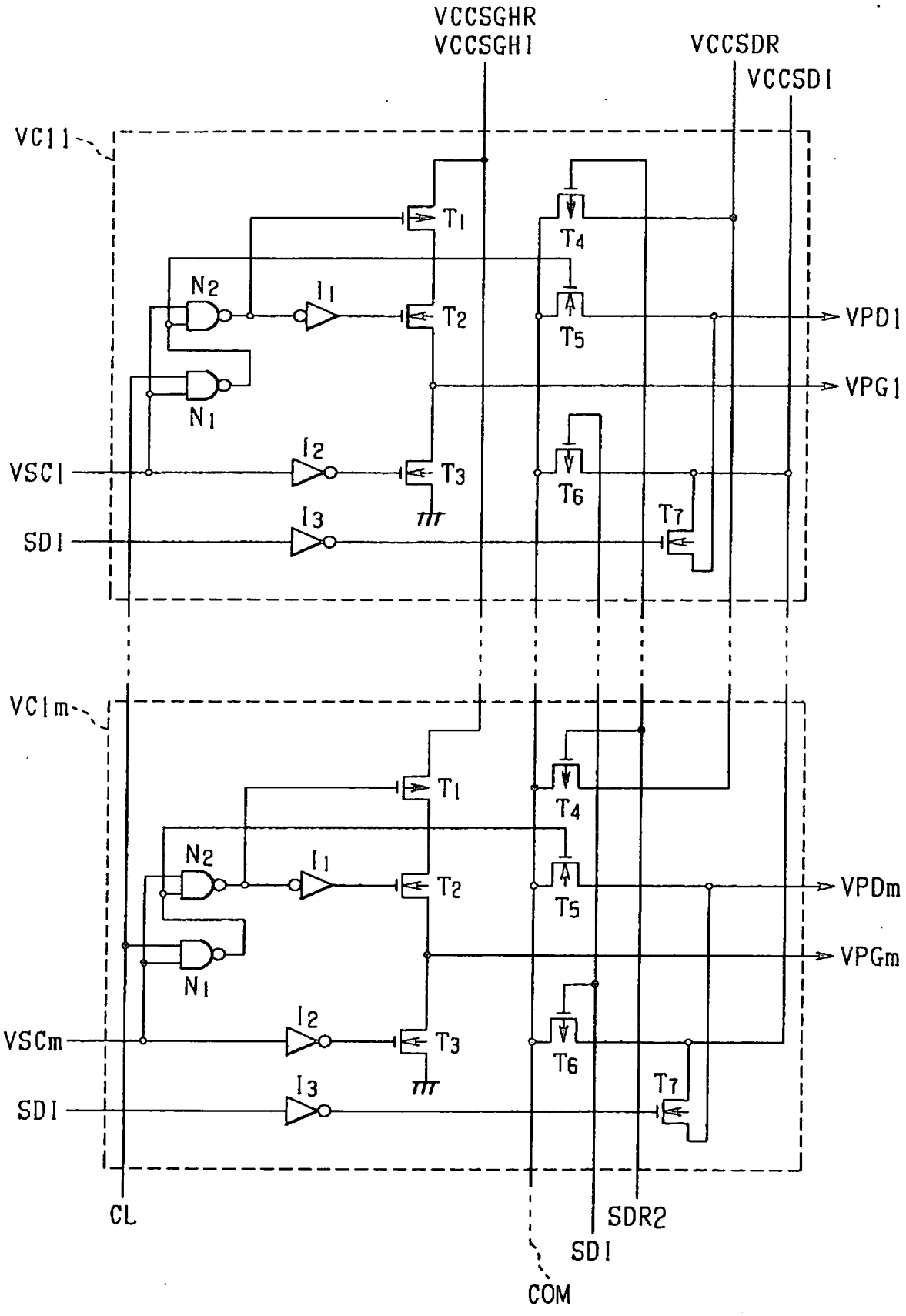
VCCSGHR
VCCSGHI
VCCSDR
VCCSDI
VC11
VC1m
T1
T2
T3
T4
T5
T6
T7
N1
N2
I1
I2
I3
VSC1
VSCm
SDI
VPD1
VPDm
VPG1
VPGm
CL
SDR2
SDI
COM

FIG. 3

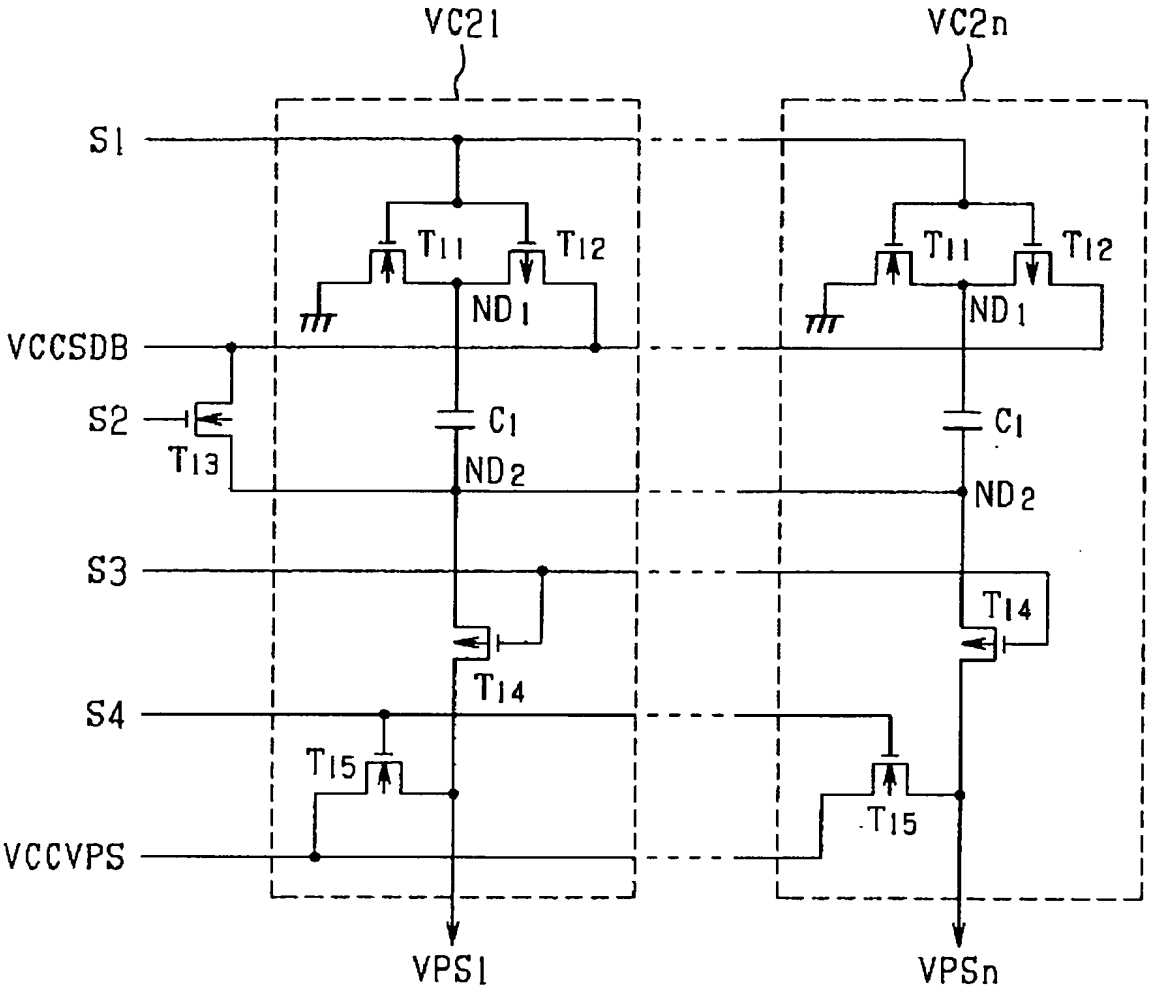
VC21
VC2n
S1
T11
T12
ND1
VCCSDB
S2
T13
C1
ND2
S3
T14
S4
T15
VCCVPS
VPS1
VPSn

FIG. 4A

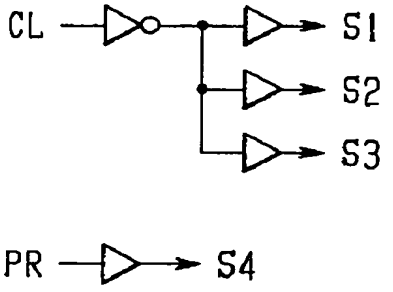
CL
S1
S2
S3
PR
S4

FIG. 4B

States of sensor bias

	state	accumulation	RESS	LOADS	PR	CL	RESN	LOADN
GATE	selected	VCCSGH1	Lo	VCCSGHR	VCCSGHR	VCCSGHR+ VCCSDB X 2	Lo1	VCCSGHR
	non selected		Lo	Lo	Lo	Lo	Lo	Lo
SOURCE	selected	turning "on" (VCCSD1)	VMPR	VCCSGHR-VthS	VCCVPS	VCCSDB X 2	VMPR	VCCSGHR-VthN
DRAIN	selected	VCCSD1	HiZ	VCCSDR	turning "on" (VCCVPS)	turning "on" (VCCSDB X 2)	HiZ	VCCSDR
	non selected		HiZ	VCCSDR	VCCVPS	VCCSDR	HiZ	VCCSDR

FIG. 5

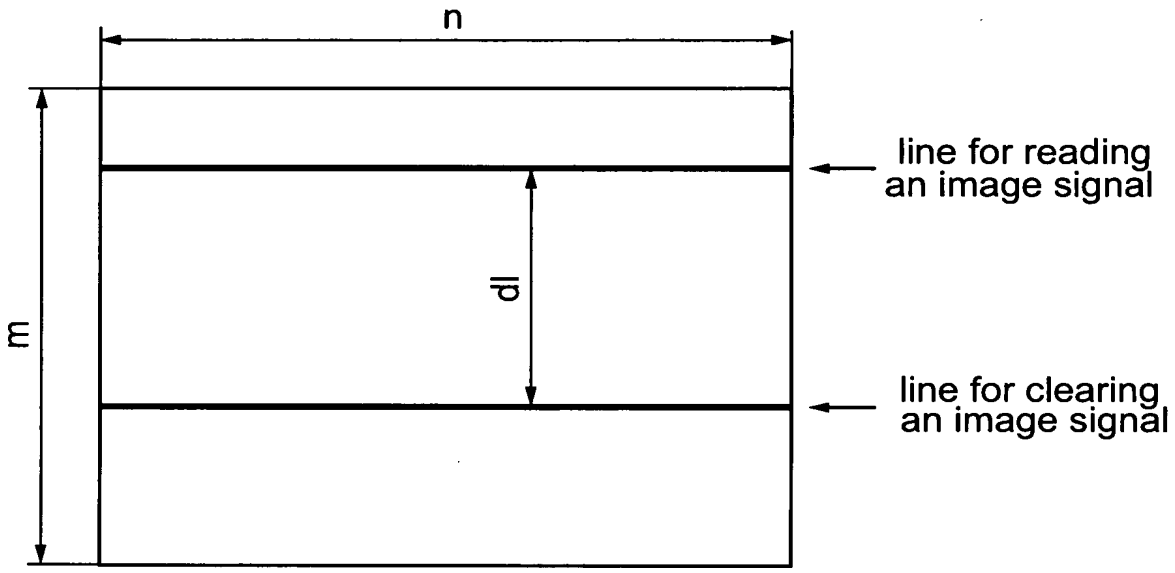
n
m
dl
line for reading an image signal
line for clearing an image signal

FIG. 6

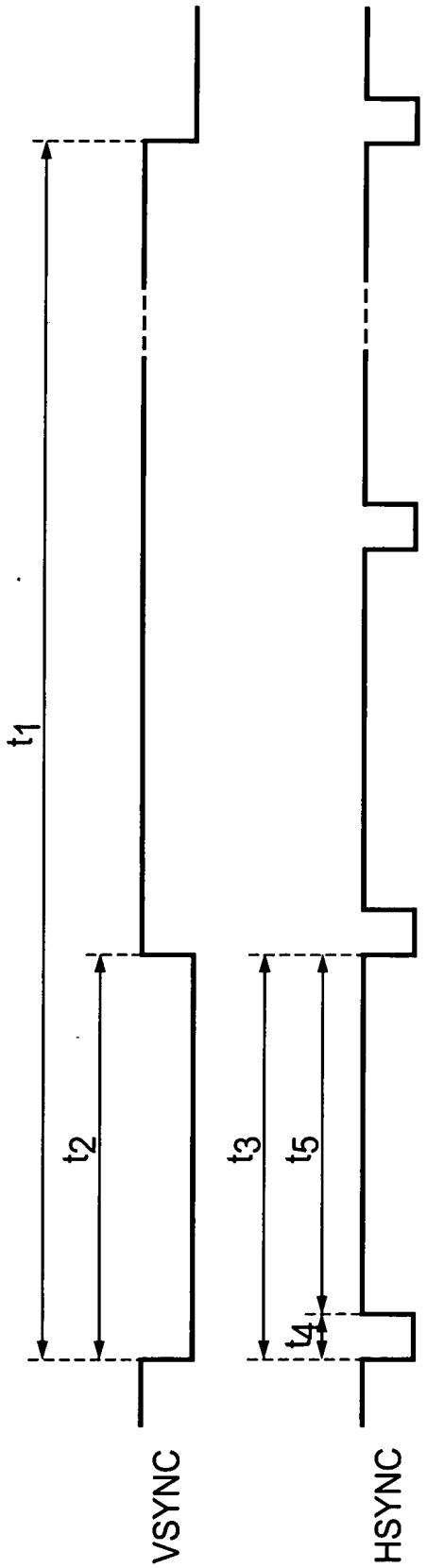

FIG. 7

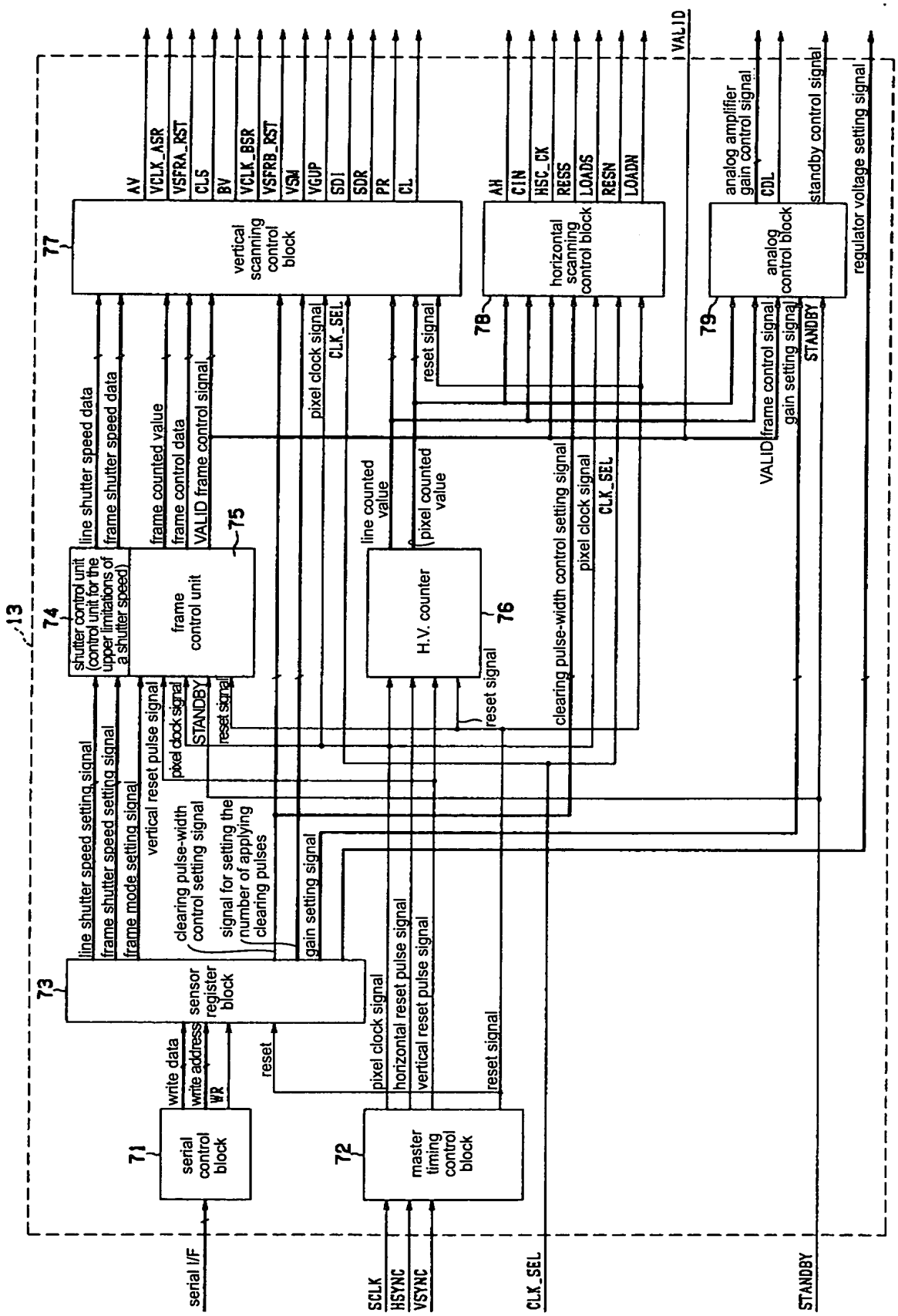
13
71
serial control block
72
master timing control block
73
sensor register block
74
shutter control unit (control unit for the upper limitations of a shutter speed)
75
frame control unit
76
H.V. counter
77
vertical scanning control block
78
horizontal scanning control block
79
analog control block
serial I/F
write data
write address
WR
reset
SCLK
HSYNC
VSYNC
pixel clock signal
horizontal reset pulse signal
vertical reset pulse signal
reset signal
CLK_SEL
STANDBY
line shutter speed setting signal
frame shutter speed setting signal
frame mode setting signal
vertical reset pulse signal
pixel clock signal
STANDBY
reset signal
clearing pulse-width control setting signal
signal for setting the number of applying clearing pulses
gain setting signal
line shutter speed data
frame shutter speed data
frame counted value
frame control data
VALID frame control signal
pixel clock signal
CLK_SEL
reset signal
line counted value
pixel counted value
reset signal
clearing pulse-width control setting signal
pixel clock signal
CLK_SEL
VALID
frame control signal
gain setting signal
STANDBY
AV
VCLK_ASR
VSFRA_RST
CLS
BV
VCLK_BSR
VSFRB_RST
VSW
VGUP
SDI
SDR
PR
CL
AH
CIN
HSC_CK
RESS
LOADS
RESN
LOADN
VALID
analog amplifier gain control signal
CDL
standby control signal
regulator voltage setting signal

FIG. 8

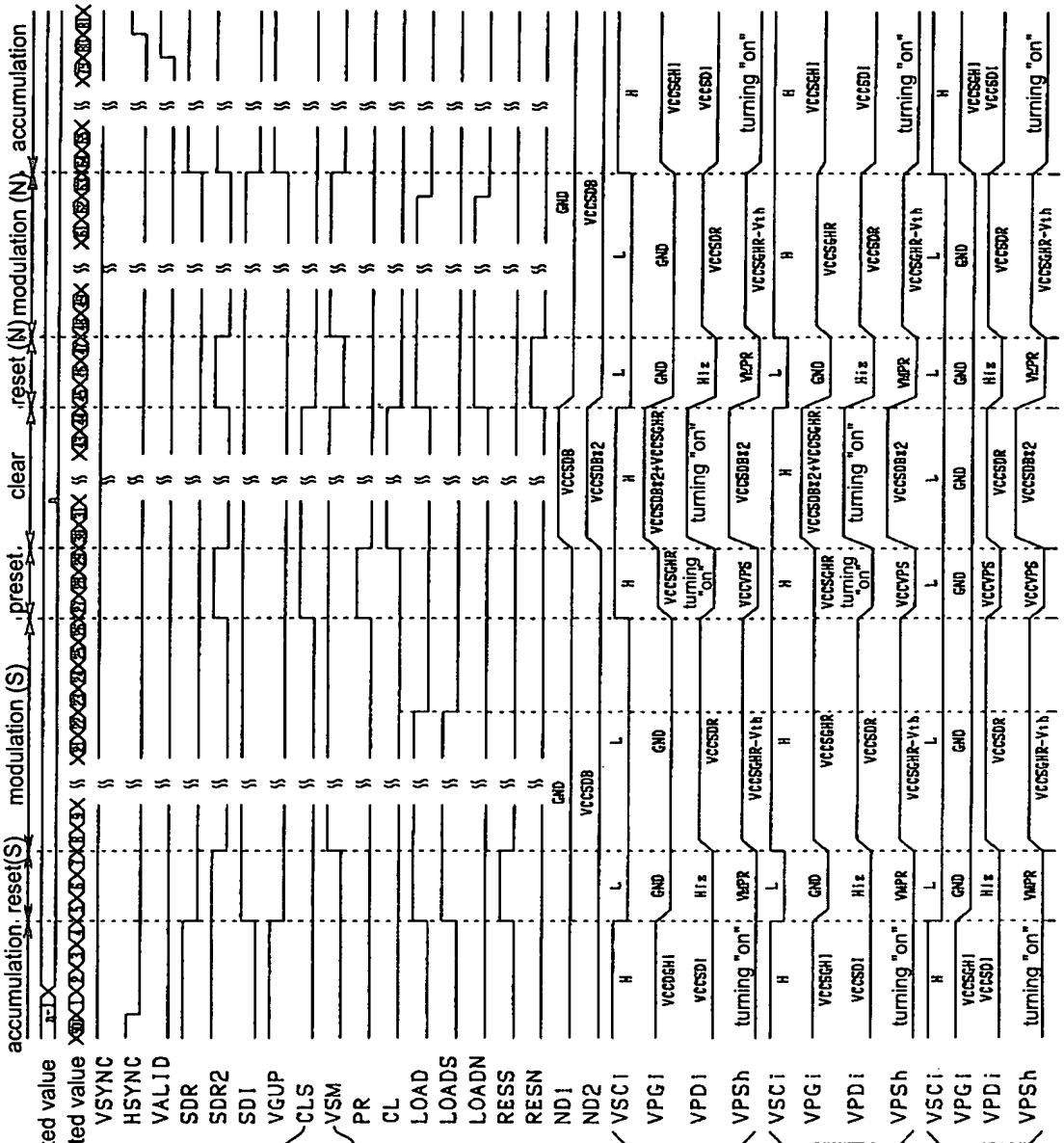
accumulation
reset(S)
modulation (S)
preset
clear
reset (N)
modulation (N)
accumulation
line counted value
pixel counted value
VSYNC
HSYNC
VALID
SDR
SDR2
SDI
VGUP
CLS
VSM
PR
CL
LOAD
LOADS
LOADN
RESS
RESN
ND1
ND2
VSCi
VPGi
VPDi
VPSh
enabling signal for selecting a line for clearing an image signal
enable signal for selecting a line for reading an image signal
a line for clearing an image signal
a line for reading an image signal
non selected line
turning "on"
GND
VCCSDB
VCCSDB2
VCCSHI
VCCSDI
VCCSDR
VCCSHR
VCCSHR-Vth
VCCVPS
VAPR
Hiz

FIG. 9

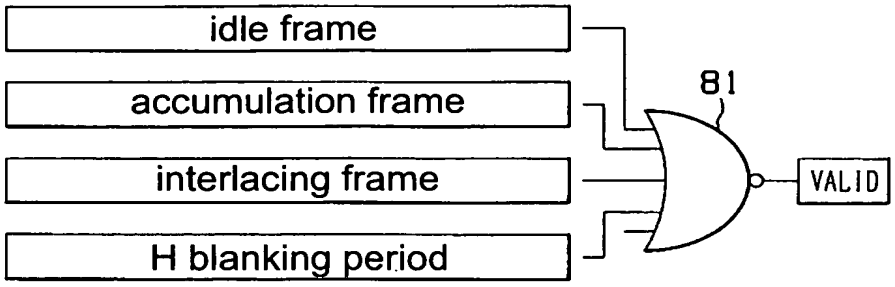

FIG. 10A

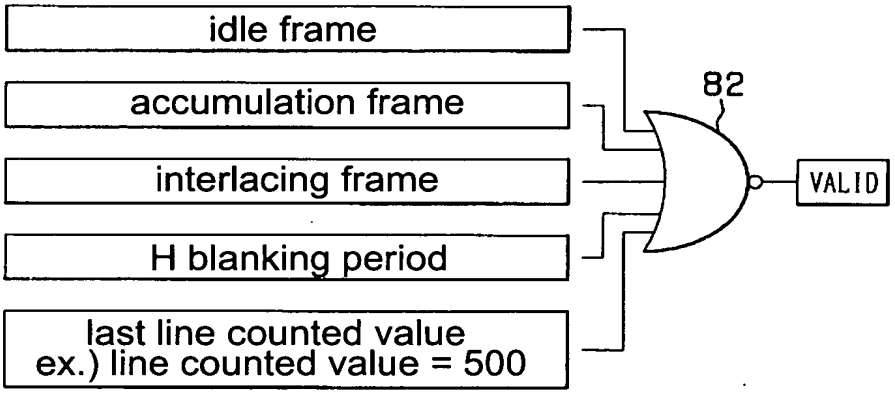

FIG. 10B

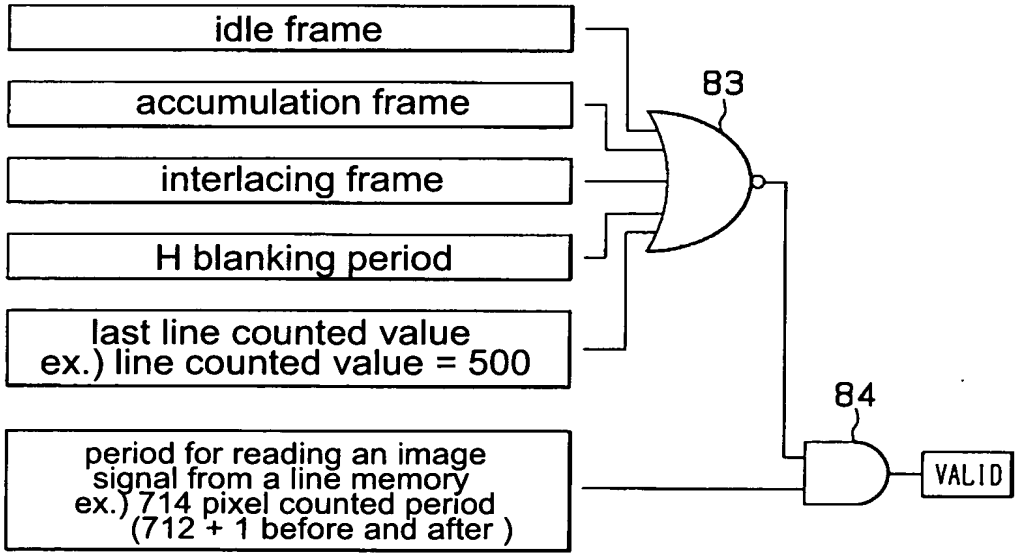

FIG. 10C

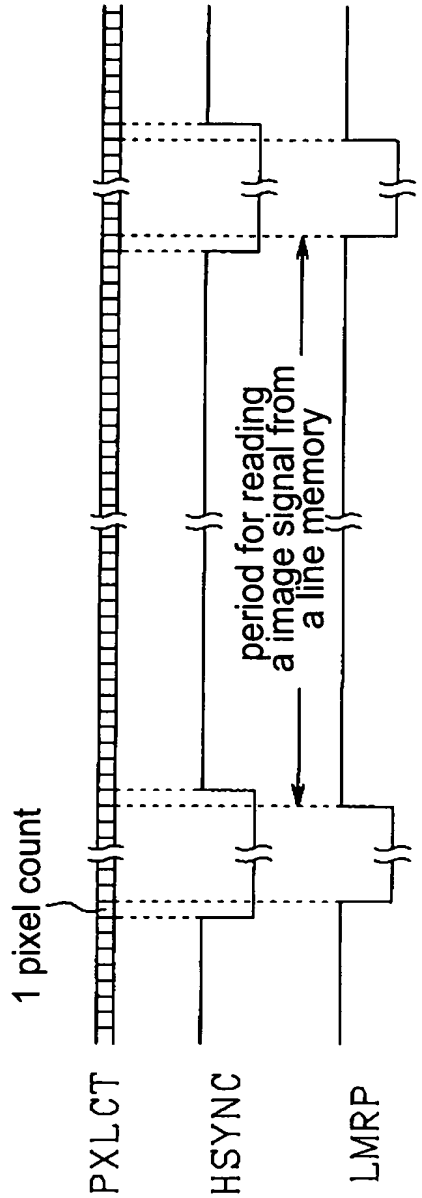
1 pixel count
period for reading
a image signal from
a line memory
PXLCT
HSYNC
LMRP

FIG. 11

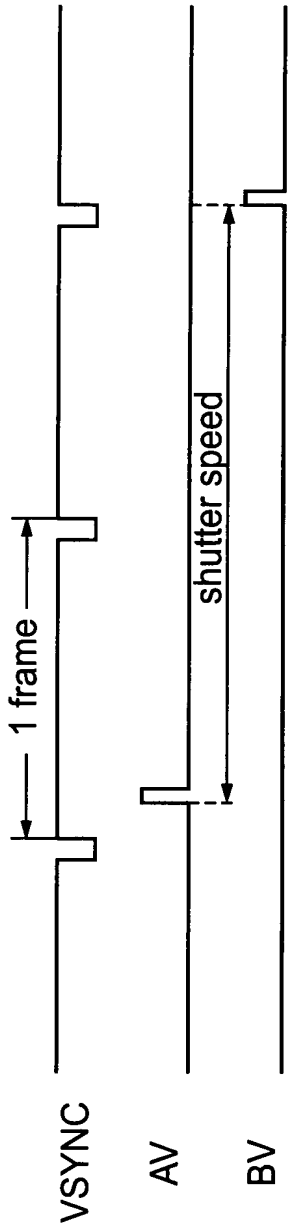

FIG. 12

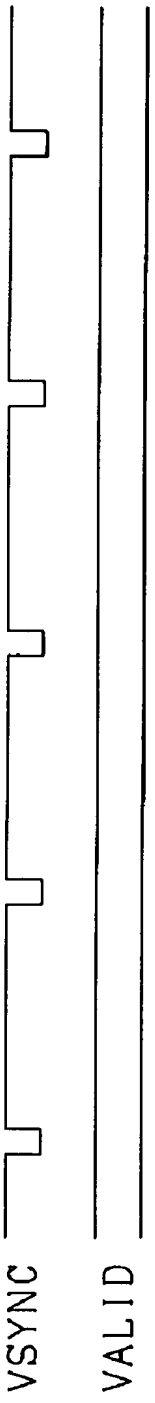

FIG. 13A

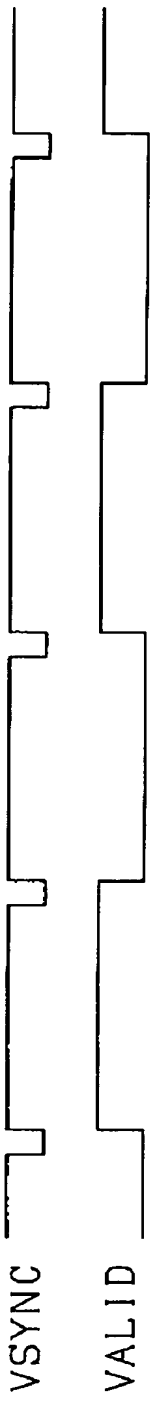

FIG. 13B

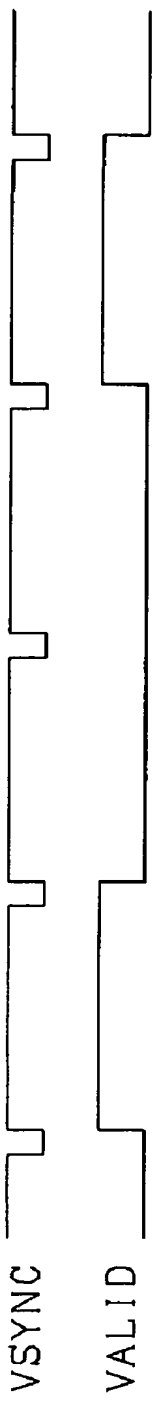

FIG. 13C